COMPUTER-AIDED DESIGN TECHNIQUES FOR MICROWAVE MONOLITHIC INTEGRATED CIRCUITS

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ABSTRACT

Thoroughly defined models of active devices that represent actual behavior, and passive structures which include parasitic effects are developed using analytical and experimental techniques. The enhanced simulations tools which incorporate them are then used in the design of MMICs. Theoretical and experimental correlation of several MMIC amplifier and mixer circuits designed to date are presented. The success of these chips is established by demonstrating a close relationship between the "designed" and "fabricated" circuits. The design techniques presented in this paper can be utilized in achieving first-pass success, and consequent 3 to 1 reduction in chip cost by minimizing the design risk.

INTRODUCTION

Microwave and millimeter-wave monolithic integrated circuits have the potential of being extensively used in future military and space communication systems such as missile seekers, smart munition, and electronic warfare [1]. The key to success depends on their insertion in various selected brassboards. Subsystems or modules consisting of several MMIC chips, or a combination of hybrid and monolithic chips in a package are required in order to realize them in a cost-effective manner. Their producibility is an increasingly important issue for high-volume applications. The complexities of circuit and its interactions with package, along with assembly and testability require a thorough understanding of yield and cost [2-5] impacts at various levels.

The threshold of MMIC chip specifications, to a certain extent, determines the yield at the module level. For instance, the use of high performance MMICs, which typically have lower yields and higher costs, reduces the cost of module assembly, rework and test because fewer iterations are required to achieve modules with consistence performance. On the other hand, by lowering chip performance specifications, we can obtain chips with higher yields and lower costs. But, in this case, the overall module cost increases substantially because they are difficult to produce with consistent performance. Therefore, for affordable modules, it is essential to have appropriate set of performance specifications for MMIC chips.

CHIP DESIGN

With considerable emphasis on producibility of monolithic microwave integrated circuits, the design methodology now consists of keeping in mind not only the performance of the circuit, but also making sure that they are manufacturable and will pass the performance window with maximum yield. The concept of manufacturing based MMIC design is crucial since it requires maintaining a balance between performance and manufacturing - referred to as producibility engineering. However, this approach requires a close relationship between the "designed" and "fabricated" circuits. This, in turn, requires accurate models of active devices and passive structures so that process tolerant circuits with improved yields can be designed. This will also reduce the number of design iterations by achieving the prescribed performance specifications in just one iteration. In other words, the FIRST-PASS success objective is realistically achievable by developing accurate simulation tools at subsystem, circuit, device and process levels in an integrated CAD based environment. The modeling activity in the MIMIC Phase I program provides

(a) experimental characterization of MESFETs, linear and nonlinear equivalent circuit models, noise parameters, and IP_3 over temperature,

(b) experimental characterization and analytical models of complex MMIC geometries,

(c) integration of models with circuit simulation programs, and database.

In this paper, we shall present techniques used to obtain accurate models of active devices that represent actual behavior and passive structures which include parasitic effects. Using enhanced simulation tools [7], we shall also demonstrate, via several examples of amplifiers and mixers, that a close relationship between the "designed" and "fabricated" circuits exists.

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CIRCUIT SIMULATION

Monolithic circuit design is accomplished using one of the many circuit simulation programs available from CAE tool vendors. These simulation tools utilize models of active devices and passive elements which are frequently used in microwave circuit designs. The models used are similar to those available in published literature, and are not particularly linked to any manufacturing process. Since accurate modeling is key to high performance MMIC designs, we present below our active device and passive structures modeling techniques; and integration of these models into existing simulation tool and design database.

Active Devices

Accurate models of MESFETs are crucial if the circuit must meet certain performance specifications. Usually, there is very little margin of error in the design. At the same time, the specifications also challenge the processing technology. Thus, success or failure of a design is greatly influenced. The MESFET device models are constantly being monitored to determine the extent of variation due to either normal process variations, equipment or any approved process change. This helps ascertain the adequacy or inadequacy of the models prior to circuit design and at the same time maintains a history of the process and their models. Extensive dc and rf measurements over different bias levels on 0.5 $\mu m \times 300\ \mu m$ MESFETs form the database which is utilized to develop linear model [6] and nonlinear model, as shown in Figs. 1 and 2, respectively. In additions, we have

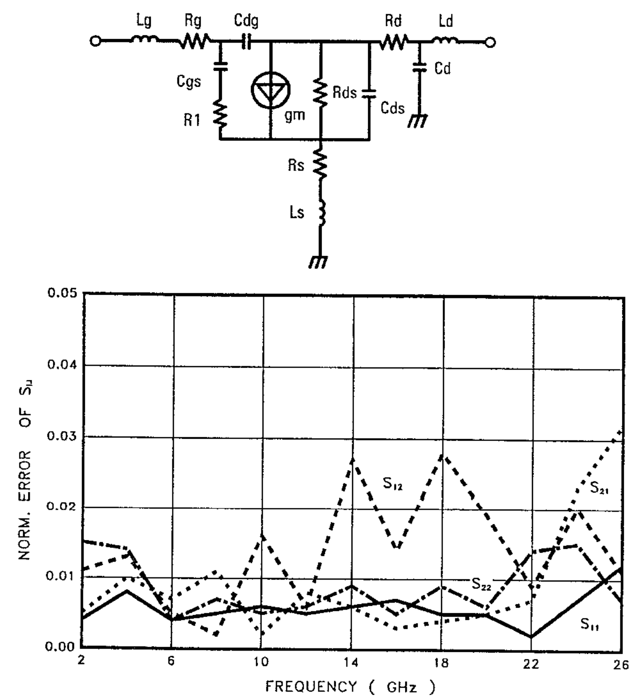


Fig. 1 Linear equivalent circuit of 0.5 × 300 μm MESFET and its accuracy.

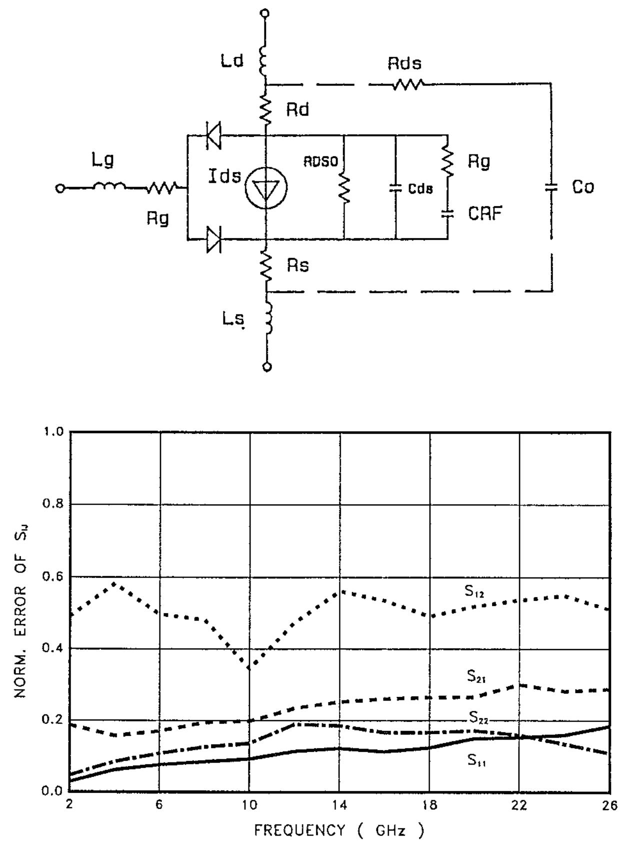


Fig. 2 Equivalent circuit of the optimized nonlinear model and its accuracy.

measured S-parameters as a function of temperature, and P_{in} and P_{out} over temperature, to develop temperature dependent models. On-wafer noise parameters of MESFETs also have been made to facilitate design of chips with particular noise specifications. The noise parameter data on F_{min}, Γ_{Opt}, and R_n are also available for optimum noise bias level.

Passive Structures

Passive structures are essential building blocks of any monolithic circuit. They can be accurately characterized using theoretical and/or experimental characterization techniques. In general, the limitation of currently used simulation tools is their accuracy beyond approximately 15 GHz. These tools may still use passive element models which are either obtained using

(a) quasi-static (TEM) approximation;

(b) field theoretic approaches under simplifying assumptions; or

(c) closed form expressions using quasi-static results.

Due to some differences in structural and process parameters, the accuracy of their models may be difficult to assess. Certain applications require passive structures for which models are not available at all. One such element is the constant-R network which is frequently used in broadband distributed amplifiers.

For first-pass success, the existing models must be improved to take into account various effects resulting from close proximity of the circuit elements such as coupling, spurious radiation, excitation of surface waves, and interactions with package modes. These aspects require special attention during circuit design and layout. Also, the accuracy of the models should be verified with theoretical and/or experimental techniques to determine their adequacy or inadequacy.

In a typical MMIC design, the circuit utilizes various process-specific and design-specific circuit structures in addition to planar microstrip discontinuity structures. They can be classified into four different catagories: lumped, distributed, interacting and special structures. In order to improve the accuracy of circuit simulations, highly accurate models of these structures are desired. A 3-inch wafer containing more than 600 elements for experimental characterization, consists of 207 lumped structures such as rectangular and circular spiral inductors and multiport MIM capacitors; 275 distributed structures including step, bend, T- and cross junctions; and 119 interacting and special structures including via holes, airbridges, and constant-R networks.

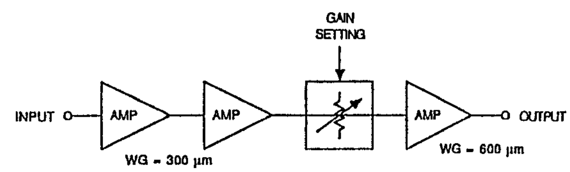
Our modeling approach aims to provide completely verified models of some planar discontinuity structures utilizing two different types of measurements to eliminate uncertainities. The test patterns are designed in a systematic manner to arrive at practical models for structural parameters frequently used in circuit designs. To that end, we perform resonance experiments to develop models at a few discrete frequencies. They are then compared with the model developed using transmission measurements to validate their accuracy. The measured resonant frequencies and S-parameters are verified with other theoretical approaches. Finally, these completely verified models are written as external programs and linked to LIBRA, a circuit simulation program [8], to facilitate their use.

MODEL VERIFICATION

In order to verify our design methodology, we considered examples of amplifiers and mixers, two most frequently used microwave components, and compared their experimental performances with theoretical simulations.

Amplifiers

The three stage amplifiers utilize lossy match topology with bridged-T attenuator for gain control, and are self biased using a FET current source. The driver stage utilizes $0.5 \times 300\ \mu m$ MESFETs. The output of the driver is connected to the AGC cell consisting of 2 MESFETs as a bridged T- attenuator. The output from the attenuator drives the final output stage which utilizes $0.5 \times 600\ \mu m$ device. It uses input lossy match configuration to provide wideband and high IP_3 characteristics. The gate bias is achieved by MESFETs configured as a constant current sources connected in series with the source of each MESFET. The device is biased at 50 % I_{dss} to provide reasonable gain and IP_3. The rf input and output ports are dc blocked by on chip capacitors. The size of 3-7 GHz amplifier is $2.09 \times 2.1\ mm^2$ and that of 6-10 GHz amplifiers is $4.705 \times 2.1\ mm^2$. The comparison of experimental and simulated performances are shown in Fig. 3. As can be seen, the simulated gain, input and output return loss of the circuits are in good agreement with the experimental data.



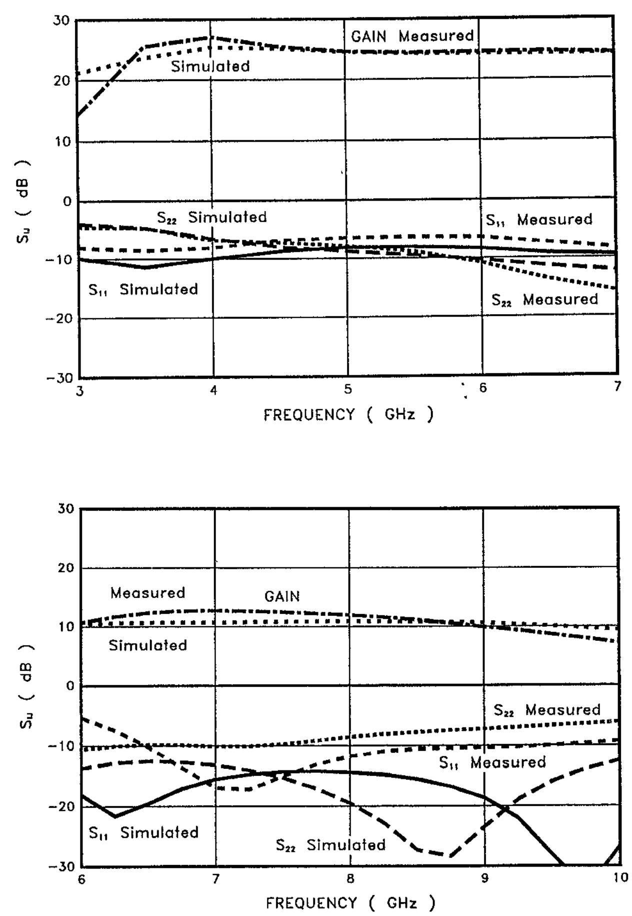


Fig. 3 Comparison of simulated and experimental performance of (a) 3-7 GHz, and (b) 6-10 GHz amplifier.

Mixers

The single balanced mixers for X- and K- bands utilize $0.5 \times 10\ \mu m$ unbiased Schottky-barrier diodes for use in medium dynamic range receiver applications. The in-phase and out-of-phase signals are obtained using a 180^o lumped element rat-race coupler. The diodes are connected between the outputs of the coupler. The IF output signal is extracted from the center connection between the two diodes. The IF signal passes through a 3 pole low pass lumped element filter and appears at the IF output. Nonlinear simulations of the circuits are performed on LIBRA utilizing a passive diode model. The measured output power with LO power of 10 dBm is plotted as a function of RF frequency. The simulated values in Fig. 4 are in good agreement with the experiments.

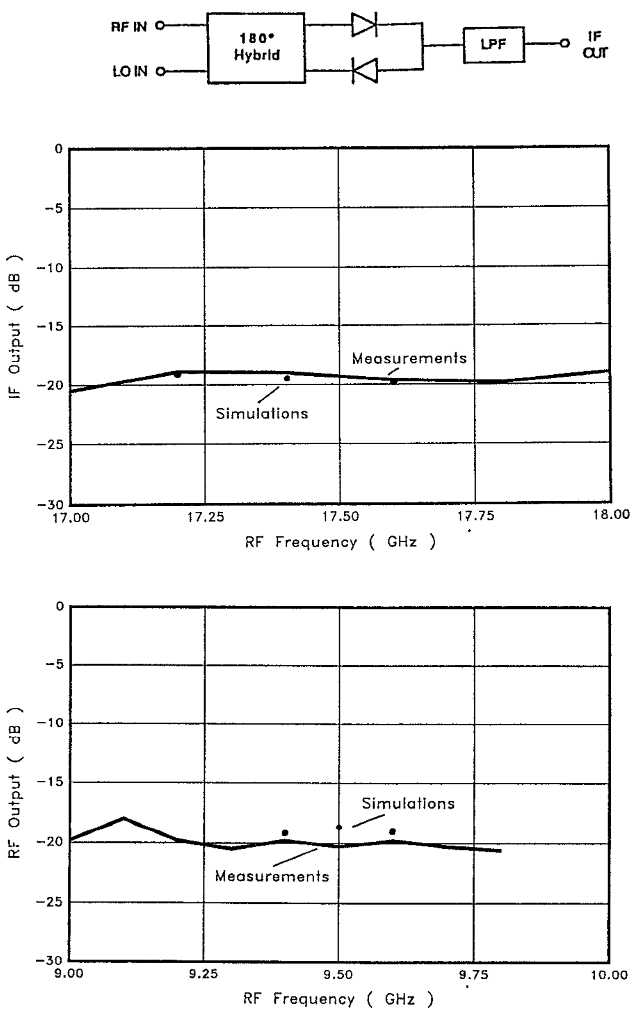


Fig. 4 Comparison of simulated and experimental performance of (a) X-band single balanced diode mixer with LO frequency = 9.9 GHz, LO power = 10 dBm, RF power = -10 dBm, and (b) K-band single balanced diode mixer with LO frequency = 18.6 to 19.6 GHz, LO power = 10 dBm, RF frequency = 17 - 18 GHz, RF power = -10 dBm, IF frequency 1.6 GHz (fixed).

CONCLUSION

In this paper we have demonstrated computer-aided design techniques incorporating accurate models of active devices and passive structures. The amplifiers and mixers designed using enhanced accuracy of circuit simulation show good correlation between the "designed" and the "fabricated" chip. This will definitely increase confidence level of designers and facilitate rapid and efficient development of a large number of high quality and high performance modules providing complex functions. Furthermore, due to reduced design risk, a 3 to 1 reduction in module cost can be achieved.

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